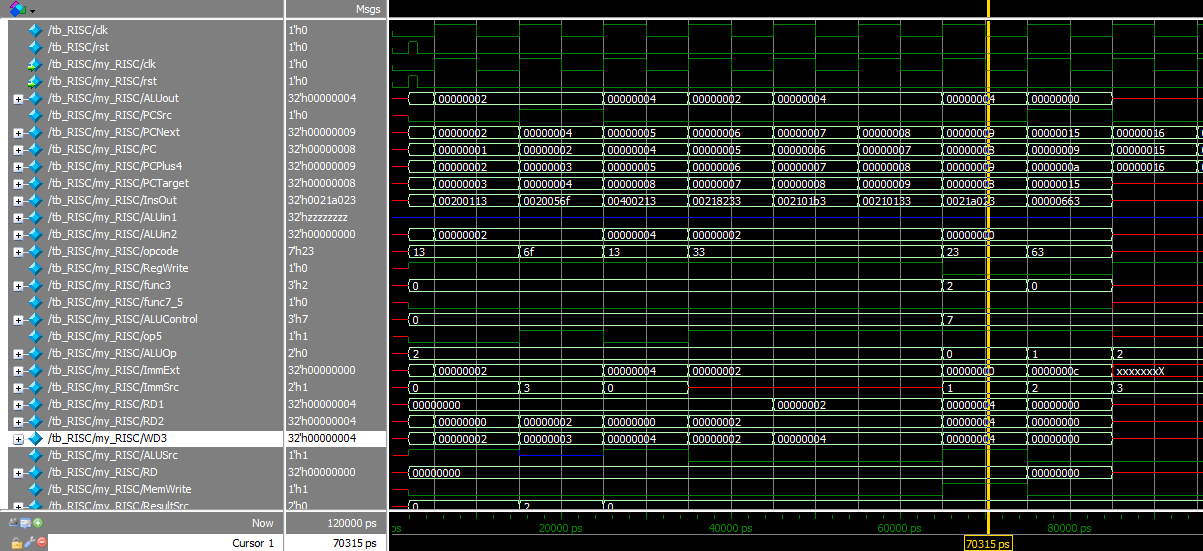
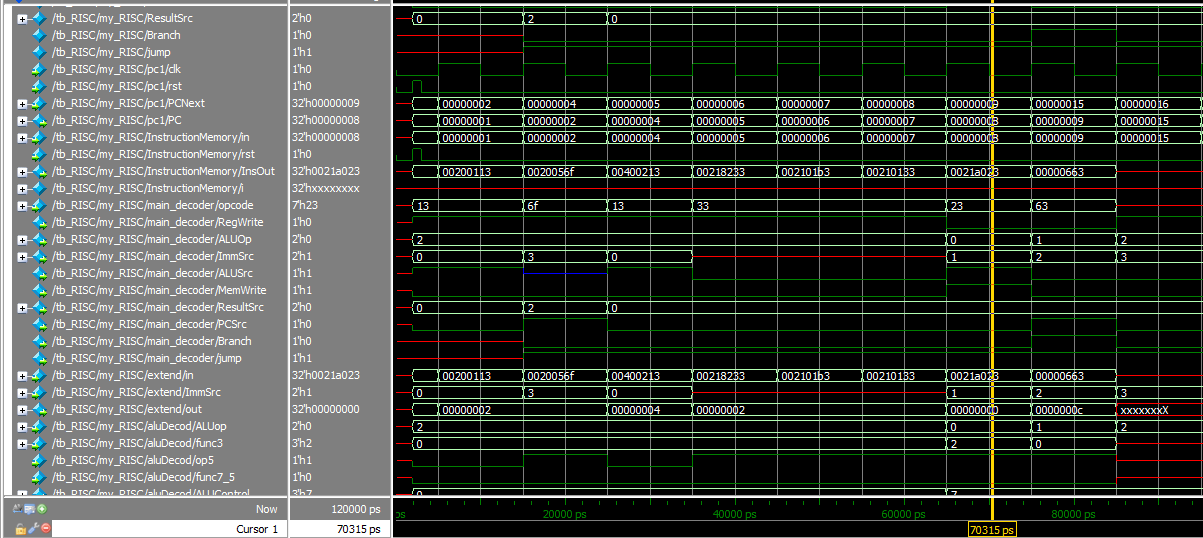
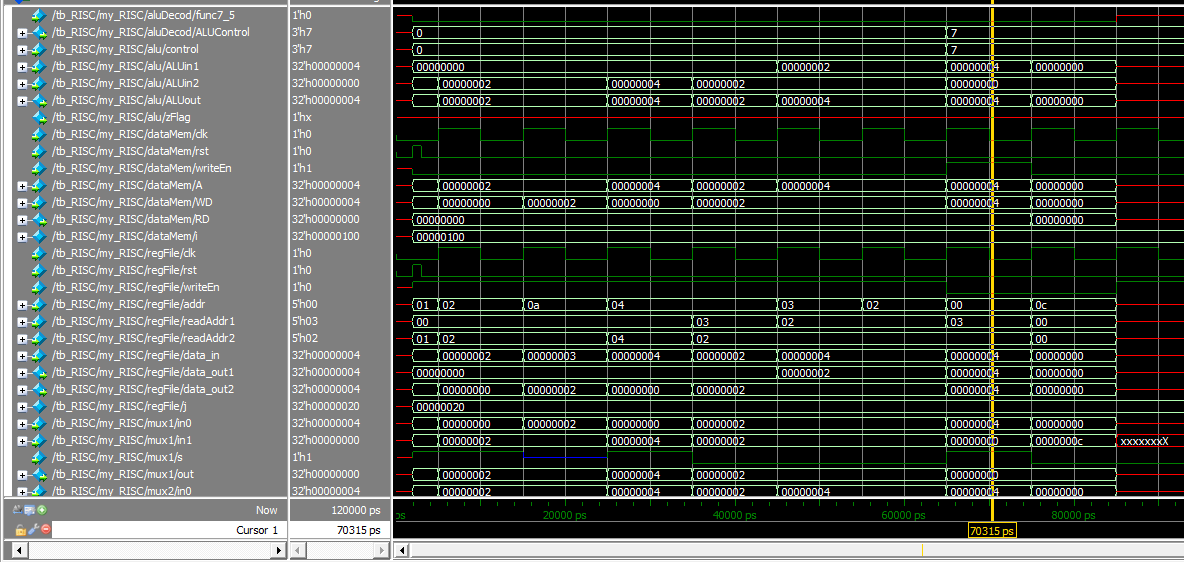
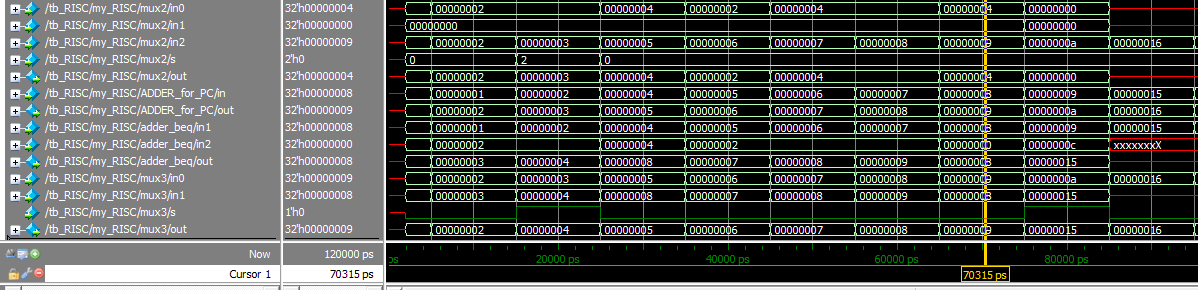
**Simulations of Single Cycle RISC-V**

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| **Assembly Code** | **MachineCode** |
| addi x1, x0, 1  addi x2, x0, 2  jal x10, 2  addi x3, x0, 3  addi x4, x0, 4  add x4, x3, x2  add x3, x2, x2  add x2, x2, x2  sw x2, 0, x3  beq x0, x0, C | 00000000000100000000000010010011  00000000001000000000000100010011  00000000001000000000010101101111  00000000001100000000000110010011  00000000010000000000001000010011  00000000001000011000001000110011  00000000001000010000000110110011  00000000001000010000000100110011  00000000001000011010000000100011  00000000000000000000011001100011 |

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